CLAIMS

We claim:

1. A stack of semiconductor dies, comprising:

a substrate including a first surface;

a first semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface;

at least one first support having a first surface and an opposite second surface,

wherein the inactive surface of the first semiconductor die and the first surface of the at least one support are attached to the first surface of the substrate laterally adjacent to each other, and the active surface of the first semiconductor die and the second surface of the at least one first support are in a common plane;

a second semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a first adhesive layer,

wherein the second semiconductor die is stacked on the active surface of the first semiconductor die and the second surface of the at least one support, is attached to the active surface of the first semiconductor die and the second surface of the at least one first support by the first adhesive layer, and does not overlap any of the bond pads of the first semiconductor die.

2. The stack of claim 1, wherein there are two same-size first supports, each adjacent to a respective one of two parallel sides of the first semiconductor die.

3. The stack of claim 1, wherein the at least one first support has a same thickness between its first and second surfaces as the first semiconductor die has between its active and inactive surfaces.

4. The stack of claim 1, wherein a side of the at least one first support is spaced from a facing side of the first semiconductor die; and further comprising:

an encapsulant material covering the first surface of the substrate and the stack of the first and second semiconductor dies, and filling a volume defined between the facing sides of the at least one first support and the first semiconductor die and the first adhesive layer.

5. The stack of claim 1, wherein the at least one first support abuts a side of the first semiconductor die.

6. The stack of claim 1, wherein the at least one first support is formed of a semiconductor material.

7. The stack of claim 1, wherein the at least one first support is formed of an elastomer film.

8. The stack of claim 1, wherein the at least one first support is attached to the first surface of the substrate by a hardened adhesive material, and a fillet of the adhesive material substantially fills a volume between facing sides of the first semiconductor die and the at least one first support.

9. The stack of claim 1, wherein the first adhesive layer comprises an elastomer film.

10. The stack of claim 1, wherein an area of the active surface of the second semiconductor die is at least equal to an area of the active surface of the first semiconductor die.

11. The stack of claim 1, further comprising:

at least one second support having a first surface and an opposite second surface,

wherein the first surface of the at least one second support is attached to the active surface of the first semiconductor die adjacent to the second semiconductor die and without overlapping any of the bond pads of the first semiconductor die, and the active surface of the second semiconductor die and the second surface of the at least one second support are in a common plane; and

a third semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a second adhesive layer,

wherein the third semiconductor die is stacked on the active surface of the second semiconductor die and the second surface of the at least one second support, is attached to the active surface of the second semiconductor die and the second surface of the at least one second support by the second adhesive layer, and does not overlap any of the bond pads of the second semiconductor die.

12. The stack of claim 11, wherein there are two same-size second supports, each adjacent to a respective one of two parallel sides of the second semiconductor die.

13. The stack of claim 11, wherein the third semiconductor die overlaps the bond pads of the first semiconductor die.

14. The stack of claim 11, wherein an area of the active surface of the third semiconductor die is at least equal to an area of the active surface of the second semiconductor die.

15. The stack of claim 14, wherein an area of the active surface of the second semiconductor die is at least equal to an area of the active surface of the first semiconductor die.

16. The stack of claim 11, wherein there is only one first support and one second support.

17. The stack of claim 11, wherein there are a plurality of first supports and a plurality of second supports.

18. The stack of claim 11, wherein the third semiconductor die is laterally offset from the first semiconductor die.

19. The stack of claim 11, wherein a centerline of the third semiconductor die overlies a parallel corresponding centerline of the first semiconductor die.

20. The stack of claim 11, wherein the third semiconductor die does not overlap the first semiconductor die.

21. The stack of claim 11, wherein there are two first supports and two second supports, and the two second supports are stacked on and have their respective first surface attached to the second surface of the two first supports.

22. The stack of claim 11, wherein the third semiconductor die does not overlap the bond pads of the first semiconductor die.

23. The stack of claim 1, further comprising:

a third semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a second adhesive layer,

wherein the third semiconductor die is stacked on the active surface of the second semiconductor die, is attached to the active surface by the second adhesive layer, and does not overlap any of the bond pads of the second semiconductor die.

24. The stack of claim 23, wherein the third semiconductor die overlaps the bond pads of the first semiconductor die.

25. A stack of semiconductor dies, comprising:

a substrate including a first surface;

a first semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface attached to the first surface of the substrate by a first adhesive layer;

a second semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a second adhesive layer,

wherein the second semiconductor die is stacked on the active surface of the first semiconductor die, is attached to the active surface of the first semiconductor die by the second adhesive layer, and does not overlap any of the bond pads of the first semiconductor die;

a third semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a third adhesive layer, wherein the third semiconductor die is attached to the active surface of the second semiconductor die by the third adhesive layer and does not overlap any of the bond pads of the second semiconductor die;

at least one first support having a first surface attached to the active surface of the second semiconductor die adjacent to the third semiconductor die, and an opposite second surface that is in a common plane with the active surface of the third semiconductor die, wherein the at least one first support does not overlap any of the bond pads of the second semiconductor die; and

a fourth semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface that is entirely covered by a fourth adhesive layer, wherein the fourth semiconductor die is attached to the active surface of the third semiconductor die and to the second surface of the at least one first support by the

fourth adhesive layer and does not overlap any of the bond pads of the third semiconductor die.

26. The stack of claim 25, wherein the first semiconductor die comprises two laterally adjacent semiconductor dies having a common semiconductor substrate.

27. The stack of claim 25, wherein the first and second semiconductor dies each comprise two laterally adjacent semiconductor dies having a common semiconductor substrate.

28. The stack of claim 25, further comprising:

at least one second support having a first surface attached to the active surface of the first semiconductor die adjacent to the second semiconductor die, and an opposite second surface that is in a common plane with the active surface of the third semiconductor die, wherein the at least one first support does not overlap any of the bond pads of the first semiconductor die, and the third semiconductor die is attached to the second surface of the at least one second support by the third adhesive layer.

29. The stack of claim 28, wherein the first semiconductor die comprises two laterally adjacent semiconductor dies having a common semiconductor substrate.

30. The stack of claim 28, wherein there are two first and second supports.

31. The stack of claim 25, wherein the fourth semiconductor die is laterally offset from the second semiconductor die.

32. The stack of claim 25, wherein there is no overlap between the fourth semiconductor die and the second semiconductor die.

33. The stack of claim 25, wherein the first, second, third, and fourth semiconductor dies are all a same size.

34. The stack of claim 25, wherein a centerline of the fourth semiconductor die is centered over a parallel corresponding centerline of the third semiconductor die.

35. A stack of semiconductor dies, comprising:

stacked first, second, and third semiconductor dies each including an active surface with at least one row of bond pads;

at least one first support and at least one second support,

wherein the first semiconductor die and the at least one first support are laterally adjacent, and are attached to a substrate surface,

wherein the second semiconductor die and the at least one second support are laterally adjacent, and are attached to the active surface of the first semiconductor die and the at least one first support without overlapping any of the bond pads of the first semiconductor die, and

wherein the third semiconductor die is attached to the active surface of the second semiconductor and the at least

one second support without overlapping any of the bond pads of the second semiconductor die.

36. The stack of claim 35, wherein active surface of the second semiconductor die is at least equal in area to the active surface of the first semiconductor die.

37. The stack of claim 36, wherein the active surface of the third semiconductor die is at least equal in area to the active surface of the second semiconductor die.

38. The stack of claim 35, wherein the active surface of the third semiconductor die is at least equal in area to the active surface of the second semiconductor die.

39. The stack of claim 35, wherein there are two first supports and two second supports.

40. The stack of claim 39, wherein the second supports are stacked on the first supports.

41. The stack of claim 35, wherein the first semiconductor die and the at least one first support have a same thickness, and the second semiconductor die and the at least one second support have a same thickness.

42. The stack of claim 41, wherein the second and third semiconductor dies include an inactive surface opposite the active surface thereof, and a respective adhesive film overlies the entire inactive surface of the second and third semiconductor dies.

43. The stack of claim 35, wherein the second and third semiconductor dies include an inactive surface opposite the active surface thereof, and a respective adhesive film overlies the entire inactive surface of the second and third semiconductor dies.

44. A stack of semiconductor dies, comprising:

a substrate including a first surface;

a first semiconductor die having an active surface with at least one row of bond pads, and an opposite inactive surface;

at least one support having a first surface and an opposite second surface,

wherein the inactive surface of the first semiconductor die and the first surface of the at least one support are attached to the first surface of the substrate laterally adjacent to each other, and the active surface of the first semiconductor die and the second surface of the at least one support are in a common plane;

a spacer having a first surface entirely covered by an adhesive layer and coupled to the active surface of the first semiconductor die and the second surface of the at least one support, and an opposite second surface; and

a second semiconductor die having an active surface with a plurality of bond pads, and an opposite inactive surface that is coupled to the second surface of the spacer, wherein the second semiconductor die overhangs at least some of the bond pads of the first semiconductor die.

45. A stack of semiconductor dies, comprising:

a substrate including a first surface; and

a stack of at least three semiconductor dies each having an active surface with bond pads and an opposite inactive surface, at least one support having opposed first and second surfaces, and at least one spacer having opposed first and second surfaces,

wherein a first level of the stack includes a first said semiconductor die and the at least one support, with the inactive surface of the first semiconductor die and a first surface of the at least one support being coupled to the first surface of the substrate laterally adjacent to each other, and the active surface of the first semiconductor die and a second surface of the at least one support being in a common plane,

wherein the inactive surface of the other semiconductor dies and the first surface of the spacer each are entirely covered by a respective adhesive layer,

wherein either the first surface of the spacer or the inactive surface of one of the other semiconductor dies is coupled by its respective adhesive layer to the active surface of the first semiconductor die and the second surface of the at least one said support, and

wherein the spacer is coupled between the active surface of one of the semiconductor dies and the inactive surface of another of the semiconductor dies, wherein the spacer does not overlap any of the bond pads of the active surface, but overhangs at least one edge of the active surface.